

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Rule 53(b) Divisional Application of S. N. 09/288,302:

Narumi OHKAWA et al.

Serial No.: NEW

Group Art Unit: 2815 (Expected)

Filed: September 25, 2001

Examiner: ORTIZ, E. (Expected)

For: SEMICONDUCTOR DEVICE HAVING BOTH MEMORY AND LOGIC CIRCUIT
AND ITS MANUFACTURE

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 CFR 1.97(b)

Commissioner for Patents
Washington, D.C. 20231

September 25, 2001

Sir:

This Information Disclosure Statement is being filed in order to comply with Applicant's duty of disclosure under 37 CFR 1.56. The documents listed on the Form PTO-1449 were made of record in parent application Serial No. 09/288,302.

The Commissioner is authorized to charge our Deposit Account No. 01-2340 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON, LLP



Sadao Kinashi
Attorney for Applicant
Reg. No. 48,075

Attorney Docket No. 990355A
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
SK/fs
Enclosure: PTO-1449

